Precision Timing Solutions

PCI Express in Automotive Applications

Precision Timing for PCI Express

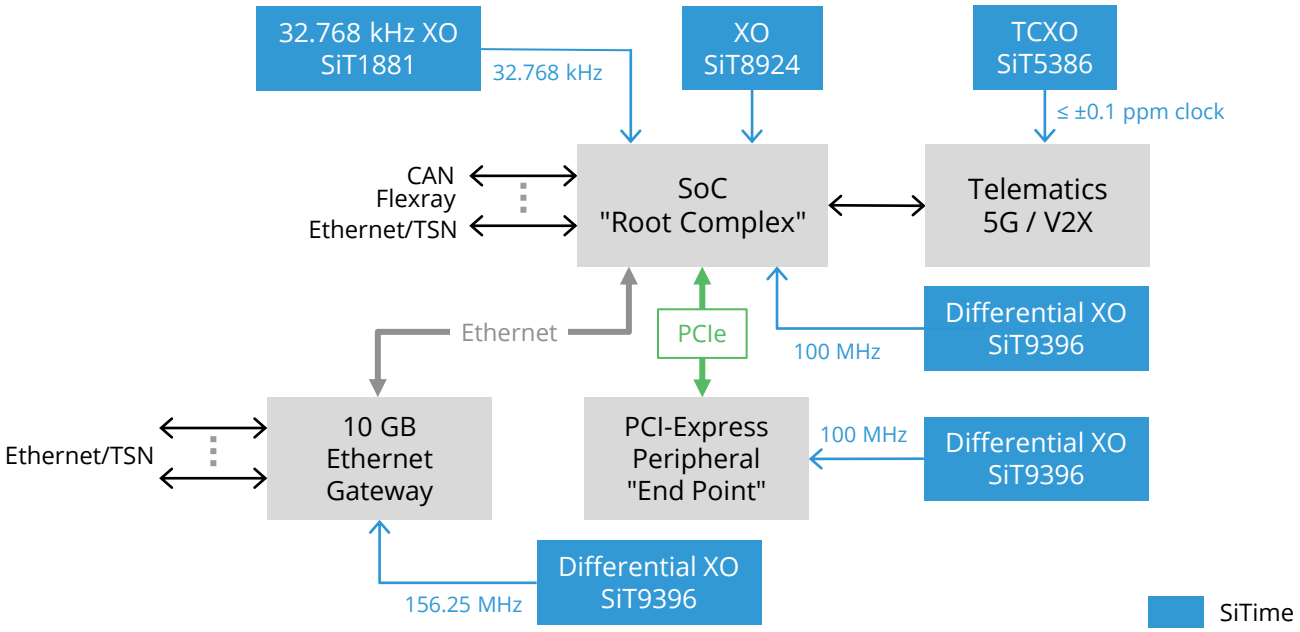
The growing demand for AD (automated driving) and ADAS (advanced driver assistance system) features in modern vehicles is driving an increase in the number and complexity of automotive electronic systems. The increasing amount of data generated by numerous sensors requires computing power. Often, a single SoC is insufficient to handle the task and coprocessors are used. PCI Express® is one of the interfaces commonly used to connect these components.

Key Considerations

- Reliability and functional safety
- High temperature
- Low jitter
- EMI reduction
- Frequency stability

PCI Express (PCIe) is a point-to-point serial interface created in 2003, originally for the computing industry. It is a bidirectional bus, based on a pair of unidirectional lanes (one in each direction). Up to 16 lanes can be aggregated in parallel to increase transfer rate. The transfer rate per lane evolved from 2.5 GT/S (GTransfer/s) with a rate of 250 MB/s per lane in PCIe Gen 1, to 64 GT/s with a rate of 7.56 GB/s in PCIe Gen 6. PCIe Gen 4 is widely used in automotive systems currently. Gen 4 features 16 GT/s, with a rate of 1.97 GB/s per lane.

The block diagram below shows an example of an automotive ECU (electronic control unit), featuring one PCIe interface:



PCIe Clocking

The PCIe interface requires a 100-MHz clock at each end of a bus. Several parameters need to be considered:

- Clock tree architecture: common clock or separate references
- Jitter, depending on the PCIe generation
- Signaling type: HCSL or LP-HCSL
- Spread spectrum for EMI reduction
- Frequency accuracy

See our PCI Express Timing Solutions in Automotive white paper for more information on jitter limits for PCIe generation, use of HCSL and LP-HCSL, spread spectrum clocking relating to PCIe, and PCIe clocking architectures.

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Featured Products – please refer to the Selector Guide for more options

Type	Product	Frequency	Key Features	Key Values
Differential oscillator	SiT9396	1 to 220 MHz	• ±30, ±50 ppm stability • LVPECL, LVDS, HCSL, Low-power HCSL, FlexSwing™ • -40°C to +125°C • 2016, 2520, 3225 packages	• High reliability • Enables interfaces with demanding jitter requirements, such as PCI-Express and 10 GB Ethernet • Supports PCIe Gen 1 to Gen 6
Clock Generator	Contact SiTime	1 to 1000 MHz	• 4 and 8 output options • ±30, ±50 ppm stability • LVPECL, LVDS, HCSL, Low-power HCSL, FlexSwing™ • Spread Spectrum • -40°C to +125°C • 4x4, 5x5 and 6x6 mm packages	• Same as above, plus: • Integration: generates PCIe as well as other clocks in the system • No external resonator needed • Please contact SiTime for information on advanced features and product availability

SiTime advantages

- Supports PCIe Gen 1 to 6; supports common clock, SRNS, and SRIS architectures.
- Clock generators feature an internal MEMS resonator and do not require an external reference.
- Silicon MEMS clock generators remove the "weak link" represented by crystal resonators. A MEMS resonator is 50x more reliable than crystal.
- The excellent reliability (< 0.5 FIT, < 0.1 DPPM) of SiTime devices makes them ideal for use in automotive and functional safety applications
- Up to 10x better resilience to shock and vibration than crystal-based devices. Shock and particularly vibration in crystals can increase the jitter of generated clocks, therefore increasing the bit error rate (BER) on a PCIe link. Shock and vibration in crystals can also create frequency micro jumps and activity dips, which degrade BER. SiTime devices are free of these problems.

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